CURRICULUM VITAE

PERSONAL INFORMATION

Name:	Vassalos Evangelos
Date of Birth:	12 October 1983, Iraklion, Crete, Greece
Current Position:	PhD Candidate (PhD Thesis Title: High Speed Arithmetic Circuits)
	Master on Electronics and Computers
	Department of Physics, University of Patras
Address:	Electronics Laboratory, Physics Department,
	University of Patras, Patras, 26500 Greece
Tel:	(Work): +30 2610 997 464
	(Mobile): +30 6937 001 815
E-mail:	vassalos@upatras.gr
Website:	http://www.ellab.physics.upatras.gr/personal/vassalos/Home.html

EDUCATIONAL BACKGROUND

2008 – Present	PhD Candidate, Electronics Laboratory, Department of Physics, University of Patras
2006 – 2008	MSc on Electronics and Computers at Department of Physics, University of Patras (MSc Deg: 8.55, with Honors)
2001 – 2006	Department of Physics, University of Patras (BSc Deg: 7,19)

SKILLS

Language Skills:	The University of Michigan: Certificate of Proficiency in English Diploma for Teaching English as a foreign Language
Computer Skills:	Microsoft Windows, Microsoft Office Suite, Visio Origin, PSPICE, Quartus, ModelSim Multisim, CCS
Programming Skills:	VHDL, Verilog, C/C++, Matlab, Fortran.

PUBLICATIONS on CONFERENSES and JOURNALS

Conference Papers

1. E. Zigouris, A. Kalantzopoulos, E. Vassalos, "LabVIEW to CCS Link for Automating Digital Signal & Image Processing Applications", In Proc. of *International Symposium on Signals, Circuits and Systems* - ISSCS 2007, vol. 2 pp. 1-4, Iasi, Romania, July 13-14, 2007, DOI: 10.1109/ISSCS.2007.4292758

2. E. Vassalos, D. Bakalis and H. T. Vergos, "Novel Modulo 2^n+1 Subtractors", In Proc. of the *16th International Conference on Digital Signal Processing* – DSP09, pp. 1-5, Santorini, Greece, 5-7 July 2009, DOI: 10.1109/ICDSP.2009.5201052

3. E. Vassalos, and D. Bakalis, "Combined SD-RNS Constant Multiplication," In Proc. of the *12th Euromicro Conference on Digital System Design, Architectures, Methods and Tools*, DSD09, pp. 172-179, Patras, Greece, 27-29 August 2009, DOI: 10.1109/DSD.2009.175

4. E. Vassalos, D. Bakalis and H. T. Vergos, "SUT-RNS Forward and Reverse Converters," *IEEE Computer Society Annual Symposium on VLSI*, ISVLSI10, pp. 11-17, Kefalonia, Greece, 5-7 July 2010 , DOI: 10.1109/ISVLSI.2010.23

5. E. Vassalos, D. Bakalis and H. T. Vergos, "On The Use Of Double-LSB And Signed-LSB Encodings For RNS," *17th International Conference on Digital Signal Processing*–DSP11, Corfu, Greece, 6-8 July 2011

6. E. Vassalos, D. Bakalis and H. T. Vergos, "Modulo 2^n+1 Arithmetic Units with Embedded Diminished-to-Normal Conversion", Proceedings of 14th Euromicro Conference on Digital System Design: Architectures, Methods & Tools (DSD), pp. 468-475, Oulu, Finland, August 31 - September 2, 2011.

Journal Papers

1. E. Vassalos, and D. Bakalis, "CSD-RNS-based Single Constant Multipliers," Journal of Signal Processing Systems, Springer, 2011. (In Press)

2. E. Vassalos, D. Bakalis and H. T. Vergos, "On the Design of Modulo $2^n \pm 1$ Subtractors and Adders/Subtractors", Circuit, Systems and Signal Processing, Springer, vol. 30, no. 6, pp. 1445-1461, December 2011.

Book Chapters

3. E. Vassalos, D. Bakalis and H. T. Vergos, "SUT-RNS Forward and Reverse Converters", VLSI 2010 Annual Symposium: Selected Papers, Lecture Notes in Electrical Engineering, vol. 105, chapter 14, pp. 231-244, Springer, 2011.

MASTER THESIS

Oct 2007 – Jun 2008	Design of a Digital System For Audio Processing, Based On NIOSII, Implemented With Altera's FPGA DE2 Board (Cyclone II Ed). Supervisor: Lector D. Bakalis, Electronics Laboratory, Dept of Physics, University of Patras

PROJECTS

Mar 2008 – Jun 2008	**Electronics for Telecommunications:** A Comparative Study of State of the Art LNA Amplifiers. Supervisor: Prof G. Kalivas, Applied Electronics Lab, Electrical Engineering Dpt.,University of Patras.
Mar 2008 – Jun 2008	**Data, Computer and GSM Networks:** GSM - Channel Concept and Call Setup, A Study on Ericsson's Systems. Supervisor: Prof S. Louvros, Electronics Laboratory, Dept of Physics, University of Patras.
Mar 2008 – Jun 2008	**Advanced Image Processing:** Neural Networks for Pattern Recognition using MATLAB. Supervisor: Prof V. Anastasopoulos, Electronics Laboratory, Dept of Physics, University of Patras.

Oct 2007 – Feb 2007   **Optical Telecommunications:**

A Study on Coarse and Dense Wavelength-Division

Multiplexing in Optical Networks.

Supervisor: Prof E. Zygouris, Electronics Laboratory,

Oct 2007 – Feb 2007   **System Design with DSPs:**

FSK - DPSK Transmitter / Receiver Implementation using

SIMULINK and two TMS320C6713 DSK Boards.

Supervisor: Prof E. Zygouris, Electronics Laboratory,

Dept of Physics, University of Patras.

Oct 2007 – Feb 2007   **System Design with DSPs:**

Design of a 3-Band Graphical Equalizer and Implementation

with LabView v7.1 on C6713 DSK.

Supervisor: Prof E. Zygouris, Electronics Laboratory,

Dept of Physics, University of Patras.

Mar 2007 – Jun 2007   **Computer Architecture and VHDL:**

Embedded System Design based on NiosII Using Quartus 7.2

and NiosII IDE & Implementation using Altera's DE2 Board.

Supervisor: Prof E. Zygouris, Lector D.Bakalis, Electronics

Laboratory, Dept of Physics, University of Patras.

Mar 2007 – Jun 2007   **Computer Architecture and VHDL:**

Designing a DSP Core in VHDL.

Supervisor: Prof E. Zygouris, Electronics Laboratory, Dept of

Physics, University of Patras.

Oct 2006 – Feb 2007   **Digital Image Processing:**

Study of Fuzzy Image Thresholding Algorithms and

Implementation with MATLAB for OCR Applications

Supervisor: Prof S. Fotopoulos, Electronics Laboratory,

Dept of Physics, University of Patras.

Oct 2006 – Feb 2007   **Digital Signal Processing:**

Study of Signal Processing Algorithms (DFT, FFT, DCT, FIR/IIR Filtering) and Implementation with MATLAB.

Supervisor: Prof S. Fotopoulos, Electronics Laboratory, Dept of Physics, University of Patras.

Mar 2006 – Jun 2006   **Analog Integrated Circuits:**

Design of Analog Filters (Chebyshev, Butterworth, Complex filters, RLC) and VLSI (layout) implementation.

Supervisor: Prof C. Pcychalinos, Electronics Laboratory, Dept of Physics, University of Patras.

Feb 2005 – June 2005   **Microprocessors II:**

Implementation of Microcomputer System Based on Intel's 8085 microprocessor.

Supervisor: Prof E. Zygouris, Electronics Laboratory, Dept of Physics, University of Patras.

Nov 2004 – Dec2004   **Microprocessors I:**

Multiplication and Division of Signed and Unsigned 16-bit Numbers using Intel's 8085 microprocessor (assembly).

Supervisor: Prof E. Zygouris, Electronics Laboratory, Dept of Physics, University of Patras.

Nov 2004 – Dec 2004   **Digital Electronics Laboratory:**

VGA Synchronization Signal Generation in VHDL for Altera's CPLD (FLEX10K) UP1 Board .

Supervisor: Prof E. Zygouris, Electronics Laboratory, Dept of Physics, University of Patras.

Oct 2004 – Oct 2005   **Final Year (Undergraduate) Thesis :**

Interfacing the OV7620 CMOS Colour Image Sensor to the TMS320C6711 DSP Module.

Supervisor: Prof E. Zygouris, Electronics Laboratory,

PROFESSIONAL / EDUCATIONAL EXPERIENCE

Oct 2011 – Jen 2012	Professor Assistant in "Programming Labs I", Dept. of
Oct 2010 – Jen 2011	Physics, University of Patras
Oct 2009 – Jen 2010	Professor Assistant in "Digital Electronics Laboratory",
Oct 2008 – Jen 2009	Dept. of Physics, University of Patras
Oct 2007 – Jen 2008	
Mar 2012 – Jun 2012	Professor Assistant in "Programming Labs II", Dept. of
Mar 2011 – Jun 2011	Physics, University of Patras
Mar 2010 – Jun 2010	Professor Assistant in "Electronics Labs I", Dept of Physics,
Mar 2009 – Jun 2009	University of Patras
Mar 2008 – Jun 2008	
Mar 2007 – Jun 2007	

RESEARCH INTERESTS

Residue and Redundant Number Systems

High-Speed Arithmetic Circuits

Digital System Design using VHDL/Verilog

Digital VLSI Design

DSP Embedded Systems

HONOURS - SCOLARSHIPS

1. Member of The World Student Organizing Committee for the "Education Without Borders 2009" Conference In Dubai UAE, As Representative of Greece and the University of Patras

2. Ph.D research Funding Program "Constantin Carathéodory", by University of Patras Duarion: 01/2010–12/2012 (36 months), Supervisor: Assistant Prof. D.Bakalis, Physics Department, University of Patras

REFERENCES

Assistant Professor E. Zygouris
Department Department of Physics, University of Patras, Greece

Tel: +30 2610 997 465
Email: ez@physics.upatras.gr

Associate Professor D.Bakalis
Department of Physics, University of Patras, Greece

Tel: +30 2610 996 287
Email: bakalis@physics.upatras.gr

Assistant Professor H. T. Vergos
Computer Engineering and Informatics Department, University of Patras, Greece

Tel: +30 2610 996 624
Email: vergos@ceid.upatras.gr

Professor A.Skodras
Digital Systems Department, Hellenic Open University, Greece

Tel: +30 2610 367 522
Email: skodras@eap.gr