Curriculum Vitae

Spiros Vlassis

Key Words **Analog/RF IC design, WLAN Transceivers**

Personal Information

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Short CV

Spiros Vlassis received his B.Sc.(1994) in Physics, the M.Sc.(1996) in Electronics and his Ph.D. (2000), from Aristotle University of Thessaloniki, Greece.
After PhD he worked as a senior engineer for VC-funded startup companies in the development and commercialization of high-performance RFICs for wireless communications and RF MEMS sensors for consumer applications.
He has one US patent and has published over 40 papers in journals and conferences. He is currently assistant professor in Electronics Laboratory, Department of Physics, University of Patras, Greece.
He is a member of Analog Integrated Circuits Design group of the Electronics Laboratory.(http://www.ellab.physics.upatras.gr/content/view/180/182/lang,english/)
He is representative of the Electronics Laboratory to Hellenic Semiconductor Industry Association. (http://www.hsia.gr/)
He is manager for the actions under the Program Phase-2 ¨ Support Greek Technology in microelectronics cluster" in the financing of the general secretariat research and technology.(http://www.corallia.org/en/events-a-news/calls-for-proposals/13--l-2-r.html).

Education

1996-2000 **PhD**

Thesis title: *"Design of analog non-linear integrated circuits for signal processing"*

The purpose of this work was to design non-linear integrated circuits for signal processing. It was divided into two thematic sections. The first part dealt with the classical nonlinear circuits. A low-voltage supply multiplier circuit was designed and fabricated based on transistors operating in the linear region. Also basic voltage and current-mode non-linear circuits, such as squarers, multipliers, squaring-root circuits, were proposed based on floating-gate MOS transistors. The second part dealt with the design of a nonlinear filter using analog circuits. The non-linear filters are widely used in audio and image processing. Min/max, medium and generalized-order statistics filters, were proposed based on the exclusive use of analog circuits. These filters are suitable for parallel processing of photosensor's array signals without A/D converters.

1994-1996 **M.Sc. in Electronics**

Thesis title: *"Pressure sensors interfacing circuits".*

1990-1994 **BSc in Physics**

IC Engineering professional experience

7/2006 – currently **Assistant professor**

University of Patras, Physics Dept., Electronics Laboratory

8/2006–2/2008 **Independent technical consultant**

Involved in designs, development and manufacturing of micro-electro-mechanical systems (MEMS). The products are integrated electronics and micromechanical elements on silicon wafers and computer chips. Involved also in the development of integrated TCXO based on MEMS devices and RF front-end modules (FEMs).

Design experience includes:

- ALC loops (CMOS, BiCMOS)
  - Automatic level-control loops for VCO (1.8GHz) amplitude stabilization. Noise impact and stability performance were optimized.
- Mathematical function generator circuits (BiCMOS)
  - Precision polynomial current generator for RF power amplifier linearity improvement.
- Voltage regulators (CMOS)
  - Low-drop-out (LDO) regulator for VCO's (1.8GHz) power driving. Noise reduction using by-pass capacitor was achieved. Internal stabilization capacitor was used.
- Frequency divider with programmable consumption (CMOS)
  - Low-jitter frequency divider for MEMS based oscillator. It was used to divide the RF prescaler output frequency. The current consumption was programmable in relation to the input frequency.
- Voltage and current references
- Signal detectors/indicators (BiCMOS, CMOS)
  - Power detectors. Usage of signal squaring circuitry for power detection application suitable for AGC loops. The AGC loop forces the VGA's composite rms output to a predetermined level.
  - RF envelop detectors for wireless receiver and Front-end modules (FEMs). The differential signal is rectified on the common-emitter node of a differential pair.
- Phase interpolator (Verilog)
  - Phase interpolator for frequency trimming of MEMS-based oscillator.
- OPAMP design for many applications (CMOS,BiCMOS).
  - Applications: low voltage; low offset; high-frequency.

9/2001- 6/2006 **Senior IC Engineer, "Theta Microelectronics", Athens, Greece.**

Involved in the development of several highly integrated direct-conversion and IF-conversion single-chip transceiver ICs with integrated synthesizer which targeted the 2.4 and 5 GHz wireless LAN markets.

Design experience includes:

- Programmable AGC loops (BiCMOS)

- Fast AGC loops used in the RX path of a dual-band single-chip RF receiver operating in the 2.4 and 5 GHz bands for the following standards: 802.11a/b/g and 802.11j.

- DC-Servo calibration loops (CMOS, BiCMOS)
  - An analog DC-servo calibration loop was implemented to cancel the DC offsets and the LO leakage in the RF direct conversion receiver.
  - A digital DC-servo calibration loop for the calibration of the equivalent input voltage offset of a transmitter RF front-end was implemented.
  - Mismatch compensation loops for trimming the effect of mismatches. These loops were used to improve the accuracy of power detectors and AGC loops
- ALC loops (CMOS, BiCMOS)
  - Automatic level control loops for VCO (5 GHz) amplitude stabilization. Noise impact and stability performance were optimized.
- Multiple bands MOSFET-C integrated filters (CMOS)
  - Channel-select low-pass filters (LPF) with an n^{th}-order low-pass Chebyshev response suitable for WLAN receivers. The cut-off frequency was easily varied using MOS switches and automatically tuned to compensate for temperature and process variation.
- Automatic control circuits (CMOS)
  - Automatic tuning block for temperature and process compensation of MOSFET-C channel-select filters..
  - Automatic-tuning block for temperature and process compensation of Gm-C filters.
- Variable Gain Amplifiers (CMOS,BiCMOS)
  - A linear-in-dB VGA was implemented using a tunable-transconductor stage followed by a transresistance amplifier.
  - A linear-in-dB VGA based on an R2R ladder for input signal attenuation was implemented.
  - A linear-in-dB VGA based on adequately overlapping differential input stages was implemented.
- Mathematical function generator circuits (BiCMOS)
  - Precision voltage squaring circuit with excellent stability over PVT corners was designed which it was used for power detectors.
  - Precision exponential current generator was designed which it was used for linear in dB gain-control circuitry and Log Amplifiers.
- Voltage regulators (CMOS)
  - Low-drop-out (LDO) regulator for VCO's power driving. Noise reduction using bypass capacitor was achieved.
- Voltage and current references
- Signal detectors/indicators (BiCMOS, CMOS)
  - Power detectors. Usage of signal squaring circuitry for power detection application suitable for AGC loops.
  - RSSI for wireless receivers.
  - Logarithmic amplifiers.
- TCXO driver (CMOS)
  - Driver for a crystal oscillator, which included an envelop-stabilization loop and temperature-compensation loop.
- OPAMP design for many applications (CMOS,BiCMOS).
  - Applications: low voltage; low offset; high-frequency.

Research Projects

1996-1998	ASIC design for smart sensor interfacing circuit, Aristotle university of Thessaloniki, financing of the general secretariat research and technology.
2006-2007	Frequency synthesizer for UWB receiver, University of Patras, Greece, financing of the general secretariat research and technology.
2009-2010	RF LNA design methodology, University of Patras, Greece.

2009-2012	Innovated sensors systems development with distributed intelligence MEMsense. (Financing by Corallia, National resource, European Regional Development Fund 2007-2013, project no. 84009, MICRO-49/ E-II-A)
2009-2012	Next generation millimeter wave radio-link , -NextGenMiliWave (Financing by Corallia, National resource, European Regional Development Fund 2007-2013, project no.84702 MICRO-49/ E-II-A)

IC research fields

- Companding filters
  - Basic analog building blocks as integrators, differentiator and log-square-root-domain filters.
- Bulk-driven analog building blocks
  - Wireless receiver's back-end based on the MOS bulk-driven approach using ultra low supply voltage (1V to 0.5V). Included: channel select filters, VGA, AGC loops and DC servo loops.
- Floating-gate MOS circuits
- Analog non-linear building blocks
  - Multipliers, power detectors, square-rooting circuits.
- Analog non-linear CMOS filters for image processing
- Interfacing IC for smart pressure sensors
- Programmable class AB CMOS output stages

Proposed Research Projects

3/2009	RF Front-end CMOS for 4G multi-standard compatibility with power management. Physics Dept. University of Patras, Greece.
3/2009	Fractional Synthesizer for 4G multi-standard compatibility, collaboration of Physics Dept. and Electrical Engineering Dept., University of Patras, Greece.
1/2010	RFID based wireless sensors network for mechanical stress monitoring, collaboration of Physics Dept., Electrical Engineering Dept., University of Patras, National center for Scientific research (NCSR) "Demokritos" Institute of Microelectronics and Technological institution of Piraeus.

IC design Software

SpectreRF, ADS, Cadence layout/schematic editor

Cadence physical verification tools (DIVA, ASSURA)

Verilog A

Patent

Wireless transmitter DC offset recalibration
United States Patent Application 20060099917

Kind Code A1
Inventors: Papathanasiou; Konstantinos; (Athens, GR) ; Vlassis; Spyridon; (Athens, GR) May 11, 2006
Serial No.: 269987, Series Code: 11, Filed: November 9, 2005

Research Collaborations

- Electronic Laboratory, Dept. of Physics, Aristotle University of Thessaloniki.
- Applied Electronics Laboratory, Dept. of Electrical Engineering Dept., University of Patras
- National center for Scientific research (NCSR) “Demokritos” Institute of Microelectronics
- Electronics Department, Technological institution of Piraeus.

Publications

International Journals

International Journal and Conferences

П1. Analogue squarer and multiplier based on floating-gate MOS transistors
Vlassis, S.; Siskos, S.;
Electronics Letters
Volume 34, Issue 9, 30 April 1998 Page(s):825 - 826

П2. Analog implementation of fast min/max filtering
Siskos, S.; **Vlassis, S**.; Pitas, I.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on]
Volume 45, Issue 7, July 1998 Page(s):913 - 918

П3. Pressure sensors interfacing circuit with digital output
Vlassis, S.; Laopoulos, Th.; Siskos, S.;
Circuits, Devices and Systems, IEE Proceedings
Volume 145, Issue 5, Oct. 1998 Page(s):332 - 336

П4. CMOS analogue median circuit
Vlassis, S.; Siskos, S.;
Electronics Letters
Volume 35, Issue 13, 24 June 1999 Page(s):1038 - 1040

П5. Analog implementation of an order-statistics filter
Siskos, S.; **Vlassis, S**.; Pitas, I.;
Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on]
Volume 46, Issue 10, Oct. 1999 Page(s):1296 - 1300

П6. An interfacing circuit for piezoresistive pressure sensors with frequency output
S. Vlassis; S. Siskos
International Journal of Electronics,
Volume 87, Issue 1 January 2000, pages 119 - 127

П7. Analog implementation of erosion/dilation, median and order statistics filters **S.Vlassis,** K.Doris, S.Siskos, I.Pitas
Pattern Recognition
Volume 33, 2000, Page(s): 1023-1032.

П8. High-speed, accurate analogue CMOS rank filter
Fikos, G.; **Vlassis, S**.; Siskos, S.;

Electronics Letters
Volume 36, Issue 7, 30 March 2000 Page(s):593 - 594

П9. A Signal Conditioning Circuit for Piezoresistive Pressure Sensors With Variable Pulse-Rate Output
S. Vlassis and S. Siskos
Analog Integrated Circuits and Signal Processing,
Volume 23, Number 2 / May, 2000 Page(s): 153-162

П10. CMOS current-mode pseudo-exponential function circuit
Vlassis, S.;
Electronics Letters
Volume 37, Issue 8, 12 Apr 2001 Page(s):471 - 472

П11. CMOS outlier rejection circuit
Vlassis, S.; Siskos, S.;
Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on]
Volume 48, Issue 7, July 2001 Page(s):910 - 914

П12. Differential-voltage attenuator based on floating-gate MOS transistors and its applications
Vlassis, S.; Siskos, S.;
Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on]
Volume 48, Issue 11, Nov. 2001 Page(s):1372 - 1378

П13. A High Performance Square-Root Domain Integrator
Costas Psychalinos and **Vlassis, S.**;
Analog Integrated Circuits and Signal Processing,
Volume 32, Number 1 / July, 2002, Pages 97-101

П14. A Novel Log-Domain Differentiator
Vlassis, S. and Costas Psychalinos
Analog Integrated Circuits and Signal Processing,
Volume 32, Number 3, September, 2002, Pages 285-287

П15. A systematic design procedure for square-root-domain circuits based on the signal flow graph approach
Psychalinos, C.; **Vlassis, S.;**
Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on]
Volume 49, Issue 12, Dec. 2002 Page(s):1702 - 1712

П16. Precision Multi-Input Current Comparator and Its Application to Analog Median Filter Implementation
S. Vlassis and S. Siskos
Analog Integrated Circuits and Signal Processing,
Volume 34, Number 3 / March, 2003 Pages 233-245

П17. On the exact realization of LOG-domain elliptic filters using the signal flow graph approach
Psychalinos, C.; **Vlassis, S.;**
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on]
Volume 49, Issue 12, Dec. 2002 Page(s):770 - 774

П18. Design of voltage-mode and current-mode computational circuits using floating-gate MOS transistors
Vlassis, S.; Siskos, S.;
Circuits and Systems I: Regular Papers, IEEE Transactions on [see also Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on]
Volume 51, Issue 2, Feb 2004 Page(s):329 - 341

П19. A Square-Root Domain Differentiator Circuit

Vlassis, S. and Costas Psychalinos
Analog Integrated Circuits and Signal Processing,
Volume 40, Number 1 / July, 2004 Pages 53-59

Π20. Low-voltage CMOS V_T extractor
Vlassis, S.; Psychalinos, C.
Electronics Letters
Volume 43, Issue 17,16 Aug 2007 Page(s) 921-923

Π21. A Floating generalized impedance converter with current feedback operational amplifier
Psychalinos C., Pal C.K., **Vlassis, S.**
International journal of Electronics and Communications,
Volume 62, 2008, Page(s) 81-85

Π22. Bulk-driven Differential voltage follower
Vlassis, S.; Raikos, G.
Electronics Letters
Volume 45, Issue 25, 3 Dec 2009 Page(s) 1276-1277

Π23. Low-voltage log-domain differentiators
Psychalinos C.; **Vlassis, S.**
Analog Integrated Circuits and Signal Processing,
Volume 63, Number / May, 2010 Pages 299-306

Π24. 0.8 V Bulk-Driven Operational Amplifier
Raikos G.; **Vlassis, S.**
Analog Integrated Circuits and Signal Processing,
Volume 63, Number 3, June 2010 Pages 425-432

Π25. Low-Voltage Bulk-Driven Input Stage With Improved Transconductance
International Journal of Circuit Theory and Applications
Raikos G.; **Vlassis, S.**
International Journal of Circuit Theory and Applications
Accepted for publication

Π26. Rail-to-rail input-stage with linearly tunable transconductance
Papageorgiou, V.; **Vlassis, S.;**
Electronics Letters
Volume: 46 , Issue: 13, 2010, Page(s): 898 – 900

International Conferences

Σ1. An interface circuit for piezoresistive pressure sensors
Vlassis, S.; Siskos, S.;
Mediterranean Electrotechnical Conference, MELECON 98.
Volume 1, 18-20 May 1998 Page(s):469 - 473 vol.1

Σ2. Analog implementation of an order statistics filter
Vlassis, S.; Siskos, S.; Pitas, I.;
Mediterranean Electrotechnical Conference, MELECON 98.,
Volume 1, 18-20 May 1998 Page(s):649 - 653 vol.1

Σ3. Analog CMOS design of the incremental credit assignment (ICRA) scheme for time series classification
Vlassis, S.; Siskos, S.; Hatzopoulos, A.; Petridis, V.; Kehagias, A.;
IEEE International Symposium on Circuits and Systems, ISCAS '98.
Volume 2, 31 May-3 June 1998 Page(s):324 - 327 vol.2

Σ4. Analog CMOS four-quadrant multiplier and divider
Vlassis, S.; **Siskos, S.**;
IEEE International Symposium on Circuits and Systems, ISCAS '99.
Volume 5, 30 May-2 June 1999 Page(s):383 - 386 vol.5

Σ5. High speed and high resolution WTA circuit
Vlassis, S.; Siskos, S.;

IEEE International Symposium on Circuits and Systems, ISCAS '99. Volume 2, 30 May-2 June 1999 Page(s):224 - 227 vol.2

Σ6. A piezoresistive pressure sensor interfacing circuit
Vlassis, S.; Siskos, S.; Laopoulos, T.;
Instrumentation and Measurement Technology Conference, 1999. IMTC/99. Proceedings of the 16th IEEE
Volume 1, 24-26 May 1999 Page(s):303 - 308 vol.1

Σ7. Analogue computational circuits based on floating-gate transistors
Vlassis, S.; Yiamalis, Th.; Siskos, S.;
IEEE International Conference on Electronics, Circuits and Systems, ICECS '99. Volume 1, 5-8 Sept. 1999 Page(s):129 - 132 vol.1

Σ8. Current-mode analogue median filter
Vlassis, S.; Siskos, S.;
IEEE International Conference on Electronics, Circuits and Systems, ICECS '99,
Volume 3, 5-8 Sept. 1999 Page(s):1353 - 1356 vol.3

Σ9. CMOS outlier rejection circuit
Vlassis, S.; Siskos, S.;
IEEE International Symposium on Circuits and Systems, ISCAS 2000.
Volume 5, 28-31 May 2000 Page(s):729 - 732 vol.5

Σ10. Current-mode non-linear building blocks based on floating-gate transistors
Vlassis, S.; Siskos, S.;
IEEE International Symposium on Circuits and Systems, ISCAS 2000.
Volume 2, 28-31 May 2000 Page(s):521 - 524 vol.2

Σ11. A floating gate CMOS Euclidean distance calculator and its application to hand-written digit recognition
Vlassis, S.; Fikos, G.; Siskos, S.;
International Conference on Image Processing, 2001.
Volume 3, 7-10 Oct. 2001 Page(s):350 - 353 vol.3

Σ12. A signal flow graph based design method for square-root domain circuits
Psychalinos, C.; **Vlassis, S.**;
IEEE International Symposium on Circuits and Systems, ISCAS 2002.
Volume 2, 26-29 May 2002, Page(s):II-209 - II-212 vol.2

Σ13. A square-root domain differentiator
Vlassis, S.; Psychalinos, C.;
IEEE International Symposium on Circuits and Systems, ISCAS 2002.
Volume 2, 26-29 May 2002 Page(s):II-217 - II-220 vol.2

Σ14. A single-chip transceiver for 802.11a and Hiperlan2 wireless LANs
Pipilos, S.; Metaxakis, E.; Tzimas, A.; **Vlassis, S**.; Sgourenas, S.; Tsividis, Y.; Varelas, T.;
IEEE Radio Frequency Integrated Circuits Symposium, RFIC 2003. 8-10 June 2003 Page(s):33 - 36

Σ15. Low-Voltage Bulk-Driven Fully Balanced Differential Opamp
G.Raikos, Vlassis S., *IEEE International Conferenence on Very Large Scale Integration,* VLSI-SoC 2008, Phodes, Page(s): 17-21.

Σ16. Low-voltage CMOS voltage squarer
Raikos, G.; **Vlassis, S**.;
Electronics, Circuits, and Systems, 2009. ICECS 2009. 16th IEEE International Conference on, 2009 , Page(s): 159 – 162

Σ17. Low-voltage differential amplifier
Raikos, G.; **Vlassis, S**.;
Electronics, Circuits, and Systems, 2009. ICECS 2009. 16th IEEE

International Conference on, 2009 , Page(s): 136 – 139

Σ18. Inductive degenerated CMOS LNA optimization techniques: comparative study
V.Papageorgiou and **S.Vlassis**,
17th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2010 (accepted for publication)

Σ19. Linearly tunable MOS transconductors based on master-slave approach
17th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2010 (accepted for publication)

Σ20. 0.8V Bulk driven Variable Gain Amplifier
George Raikos and **S.Vlassis**
17th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2010 (accepted for publication)

Citations >120