

Curriculum Vitae of Prof. Dimitris Bakalis

Personal Information

Last name : Bakalis
First name : Dimitris
Occupation : Assistant Professor
Address : University of Patras, Dept. of Physics, Electronics Lab., Patras, Greece
Office phone : +30 2610 99 6796
Fax : +30 2610 99 7456
E-mail : bakalis@physics.upatras.gr
Homepage : http://www.ellab.physics.upatras.gr/~bakalis/index_en.htm

Education

- PhD, Computer Engineering & Informatics Dept., University of Patras, Greece.
- MSc, Computer Engineering & Informatics Dept., University of Patras, Greece.
- BSEng, Computer Engineering & Informatics Dept., University of Patras, Greece.

Research Interests

- Computer arithmetic
- Digital systems design with HDLs
- Embedded systems
- VLSI testing
- Built-in self-test
- External testing
- Low power testing

Publications

International Journals

1. **D. Bakalis**, X. Kavousianos, H. T. Vergos, D. Nikolos and G. Alexiou, "*Low Power Built-In Self-Test Schemes for Array and Booth Multipliers*", VLSI Design: An International Journal of Custom-Chip Design, Simulation and Testing, Gordon and Breach Publishers, vol. 12, no. 3, pp. 431-448, 2001 (DOI: 10.1155/2001/67893).
2. E. Kalligeros, X. Kavousianos, **D. Bakalis** and D. Nikolos, "*On-the-fly Reseeding: A New Reseeding Technique for test-per-clock BIST*", Journal of Electronic Testing: Theory and Applications (JETTA), Kluwer Academic Publishers, vol. 18, no. 3, pp. 315-332, June 2002 (DOI: 10.1023/A:1015039323168).
3. X. Kavousianos, **D. Bakalis**, D. Nikolos and S. Tragoudas, "*A new Built-In TPG for Random Pattern Resistant Faults*", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 21, no. 7, pp. 859-866, July 2002 (DOI: 10.1109/TCAD.2002.1013898).
4. **D. Bakalis**, E. Kalligeros, D. Nikolos, H. T. Vergos and G. Alexiou, "*On the Design of Low Power BIST for Multipliers with Booth Encoding and Wallace Tree Summation*", Journal of Systems Architecture (JSA), Elsevier Science, vol. 48, no. 4-5, pp. 125-135, December 2002 (DOI: 10.1016/S1383-7621(02)00121-2).
5. **D. Bakalis**, K. D. Adaos, D. Lympelopoulou, M. Bellos, H. T. Vergos, G. Ph. Alexiou and D. Nikolos, "*A Core Generator for Arithmetic Cores and Testing Structures with a Network Interface*", Journal of Systems Architecture (JSA), Elsevier Science, vol. 52, no. 1, pp. 1-12, January 2006 (DOI: 10.1016/j.sysarc.2004.12.006).
6. **D. Bakalis** and H. T. Vergos, "*Shifter Circuits for $\{2^n+1, 2^n, 2^n-1\}$ RNS*", Electronics Letters (ELL), IET, vol. 45, no. 1, pp. 27-29, 1 January 2009 (DOI: 10.1049/el:20092067).
7. X. Kavousianos, **D. Bakalis** and D. Nikolos, "*Efficient Partial Scan Cell Gating for Low-Power Scan-based Testing*", ACM Transactions on Design Automation of Electronic Systems (TODAES), ACM, vol. 14, no. 2, article no. 28, March 2009 (DOI: 10.1145/1497561.1497571).
8. H. T. Vergos, **D. Bakalis** and C. Efstathiou, "*Fast Modulo 2^n+1 Multi-Operand Adders and Residue Generators*", Integration, the VLSI Journal, Elsevier, vol. 43, no. 1, pp. 42-48, January 2010 (DOI: 10.1016/j.vlsi.2009.04.002).

9. H. T. Vergos and **D. Bakalis**, "On Implementing Efficient Modulo 2^n+1 Arithmetic Components", Journal of Circuits, Systems and Computers, World Scientific, vol. 19, no. 5, pp. 911-930, August 2010 (DOI: 10.1142/S0218126610006529).
10. **D. Bakalis**, H. T. Vergos and A. Spyrou, "Efficient Modulo $2^n\pm 1$ Squarers", Integration, the VLSI Journal, Elsevier, vol. 44, no. 3, pp. 163-174, June 2011 (DOI: 10.1016/j.vlsi.2011.03.006).
11. E. Vassalos, **D. Bakalis** and H. T. Vergos, "On the Design of Modulo $2^n\pm 1$ Subtractors and Adders/Subtractors", Circuits, Systems and Signal Processing, Springer, vol. 30, no. 6, pp. 1445-1461, December 2011 (DOI: 10.1007/s00034-011-9326-5).
12. E. Vassalos and **D. Bakalis**, "CSD-RNS-based Single Constant Multipliers", Journal of Signal Processing Systems, Springer, vol. 67, no. 3, pp. 255-268, June 2012 (DOI: 10.1007/s11265-010-0552-z).
13. H. T. Vergos and **D. Bakalis**, "Area-Time Efficient Multi-Modulus Adders and their Applications", Microprocessors and Microsystems, Elsevier, vol. 36, no. 5, pp. 409-419, July 2012 (DOI: 10.1016/j.micpro.2012.02.004).
14. H. T. Vergos, **D. Bakalis** and A. Anastasiou, "Lookahead Architectures for Hamming Distance and Fixed-Threshold Hamming Weight Comparators", Circuits, Systems and Signal Processing, Springer, vol. 34, no. 4, pp. 1041-1056, April 2015 (DOI: 10.1007/s00034-014-9891-5).
15. E. Vassalos and **D. Bakalis**, "Efficient architectures for modulo 2^n-2 arithmetic units", International Journal of Electronics, Taylor & Francis, vol. 102, no. 12, pp. 2062-2674, December 2015 (DOI: 10.1080/00207217.2015.1020528).

Book Chapters

1. E. Vassalos, **D. Bakalis** and D. Nikolos, "SUT-RNS Forward and Reverse Converters", in N. Voros, A. Mukherjee, N. Sklavos, K. Masselos, M. Huebner (eds), VLSI 2010 Annual Symposium: Selected Papers (ISBN: 978-94-007-1488-5), Lecture Notes in Electrical Engineering, vol. 105, chapter 14, pp. 231-244, Springer, 2011 (DOI: 10.1007/978-94-007-1488-5_14).

International Conferences, Symposia and Workshops

1. **D. Bakalis** and D. Nikolos, "On Low Power BIST for Carry Save Array Multipliers", Proc. of 5th IEEE International On-Line Testing Workshop (IOLTW), pp. 86-90, Rhodes, Greece, July 5-7, 1999.
2. **D. Bakalis**, H. T. Vergos, D. Nikolos, X. Kavousianos and G. Alexiou, "Low Power Dissipation in BIST Schemes for Modified Booth Multipliers", Proc. of 1999 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT), pp. 121-129, Albuquerque, NM, USA, November 1-3, 1999 (DOI: 10.1109/DFTVS.1999.802877).
3. **D. Bakalis**, E. Kalligeros, D. Nikolos, H. T. Vergos and G. Alexiou, "Low Power BIST for Wallace Tree-based Fast Multipliers", Proc. of 1st IEEE International Symposium on Quality of Electronic Design (ISQED), pp. 433-438, San Jose, CA, USA, March 20-22, 2000 (DOI: 10.1109/ISQED.2000.838914).
4. **D. Bakalis**, D. Nikolos and X. Kavousianos, "Test Response Compaction by an Accumulator Behaving as a Multiple-Input Non-Linear Feedback Shift Register", Proc. of International Test Conference (ITC), pp. 804-811, Atlantic City, NJ, USA, October 1-6, 2000 (DOI: 10.1109/TEST.2000.894277).
5. **D. Bakalis**, M. Bellos, H. T. Vergos, D. Nikolos and G. Alexiou, "A Macro Generator for Arithmetic Cores", Proc. of XV Conference on Design of Circuits and Integrated Systems (DCIS), pp. 734-739, Montpellier, France, November 21-24, 2000.
6. **D. Bakalis**, D. Nikolos, H. T. Vergos and X. Kavousianos, "On Accumulator-based Bit-Serial Test Response Compaction Schemes", Proc. of 2nd IEEE International Symposium on Quality Electronic Design (ISQED), pp. 350-355, San Jose, CA, USA, March 26-28, 2001 (DOI: 10.1109/ISQED.2001.915255).
7. X. Kavousianos, **D. Bakalis** and D. Nikolos, "A Novel Reseeding Technique for Accumulator-based Test Pattern Generation", Proc. of 11th ACM Great Lakes Symposium on VLSI (GLS_VLSI), pp. 7-12, West Lafayette, IN, USA, March 22-23, 2001

(DOI: 10.1145/368122.368145).

8. **D. Bakalis**, K. D. Adaos, D. Lymperopoulos, G. Ph. Alexiou and D. Nikolos, "*EUDOXUS: A WWW-based Generator of Reusable Arithmetic Cores*", Proc. of 12th IEEE International Workshop on Rapid System Prototyping (RSP), pp. 182-187, Monterey, CA, USA, June 25-27, 2001 (DOI: 10.1109/IWRSP.2001.933858).
9. S. J. Piestrak, **D. Bakalis** and X. Kavousianos, "*On the Design of Self-Testing Checkers for Berger codes*", Proc. of 7th IEEE International On-Line Testing Workshop (IOLTW), pp. 153-157, Taormina, Italy, July 9-11, 2001 (DOI: 10.1109/OLT.2001.937835).
10. E. Kalligeros, X. Kavousianos, **D. Bakalis** and D. Nikolos, "*A new Reseeding Technique for LFSR-based Test Pattern Generation*", Proc. of 7th IEEE International On-Line Testing Workshop (IOLTW), pp. 80-86, Taormina, Italy, July 9-11, 2001 (DOI: 10.1109/OLT.2001.937823).
11. E. Kalligeros, X. Kavousianos, **D. Bakalis** and D. Nikolos, "*An Efficient Seeds Selection Method for LFSR-based Test-per-clock BIST*", Proc. of 3rd IEEE International Symposium on Quality Electronic Design (ISQED), pp. 261-266, San Jose, CA, USA, March 18-20, 2002 (DOI: 10.1109/ISQED.2002.996747).
12. G. Dimitrakopoulos, D. Nikolos and **D. Bakalis**, "*Bit Serial Test Pattern Generation by an Accumulator Behaving as a Non-Linear Feedback Shift Register*", Proc. of 8th IEEE International On-Line Testing Workshop (IOLTW), pp. 152-157, Isle of Bendor, France, July 8-10, 2002 (DOI: 10.1109/OLT.2002.1030199).
13. X. Kavousianos, **D. Bakalis**, M. Bellos and D. Nikolos, "*An Efficient Test Vector Ordering Method for Low Power Testing*", Proc. of IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 285-288, Louisiana, LA, USA, February 19-20, 2004 (DOI: 10.1109/ISVLSI.2004.1339559).
14. M. Bellos, **D. Bakalis** and D. Nikolos, "*Scan Cell Ordering for Low Power BIST*", Proc. of IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 281-284, Louisiana, LA, USA, February 19-20, 2004 (DOI: 10.1109/ISVLSI.2004.1339558).
15. M. Bellos, **D. Bakalis**, D. Nikolos and X. Kavousianos, "*Low Power Testing by Test Vector Ordering with Vector Repetition*", Proc. of IEEE International Symposium on Quality Electronic Design (ISQED), pp. 205-210, San Jose, CA, USA, March 22-24, 2004 (DOI: 10.1109/ISQED.2004.1283674).
16. M. Bellos, **D. Bakalis**, D. Nikolos and X. Kavousianos, "*Vector Repetition and Modification for Peak Power Reduction in VLSI Testing*", Proc. of 8th IEEE Workshop on Design & Diagnostics of Electronic Circuits & Systems (DDECS), pp. 160-165, Sopron, Hungary, April 13-16, 2005.
17. H. T. Vergos, **D. Bakalis** and C. Efstathiou, "*Efficient Modulo 2^n+1 Multi-Operand Adders*", Proc. of 15th IEEE International Conference on Electronics, Circuits & Systems (ICECS), pp. 694-697, Malta, August 31-September 3, 2008 (DOI: 10.1109/ICECS.2008.4674948).
18. H. T. Vergos and **D. Bakalis**, "*On the Use of Diminished-1 Adders for Weighted Modulo 2^n+1 Arithmetic Components*", Proc. of 11th Euromicro Conference on Digital System Design: Architectures, Methods & Tools (DSD), pp. 752-759, Parma, Italy, September 3-5, 2008 (DOI: 10.1109/DSD.2008.22).
19. A. Spyrou, **D. Bakalis** and H. T. Vergos, "*Efficient Architectures for Modulo 2^n-1 Squarers*", Proc. of 16th International Conference on Digital Signal Processing (DSP), Santorini, Greece, July 5-7, 2009 (DOI: 10.1109/ICDSP.2009.5201052).
20. E. Vassalos, **D. Bakalis** and H. T. Vergos, "*Novel Modulo 2^n+1 Subtractors*", Proc. of 16th International Conference on Digital Signal Processing (DSP), Santorini, Greece, July 5-7, 2009 (DOI: 10.1109/ICDSP.2009.5201088).
21. E. Vassalos and **D. Bakalis**, "*Combined SD-RNS Constant Multiplication*", Proc. of 12th Euromicro Conference on Digital System Design: Architectures, Methods & Tools (DSD), pp. 172-179, Patras, Greece, August 27-29, 2009 (DOI: 10.1109/DSD.2009.175).
22. E. Vassalos, **D. Bakalis** and H. T. Vergos, "*SUT-RNS Forward and Reverse Converters*", Proc. of IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 11-16, Lixouri, Kefalonia, Greece, July 5-7, 2010 (DOI: 10.1109/ISVLSI.2010.23).
23. **D. Bakalis** and H. T. Vergos, "*Area-Efficient Multi-Moduli Squarers for RNS*", Proc. of

13th Euromicro Conference on Digital System Design: Architectures, Methods & Tools (DSD), pp. 408-411, Lille, France, September 1-3, 2010 (DOI: 10.1109/DSD.2010.25).

24. **D. Bakalis** and H. T. Vergos, "*Diminished-One Modulo 2^n+1 Multiply-Add Circuits*", Proc. of XXV Conference on Design of Circuits and Integrated Systems (DCIS), pp. 289-294, Canary Islands, Spain, November 17-19, 2010.
25. H. T. Vergos and **D. Bakalis**, "*Area-Time Efficient Multi-Moduli Adder Design*", Proc. of XXV Conference on Design of Circuits and Integrated Systems (DCIS), pp. 295-300, Canary Islands, Spain, November 17-19, 2010.
26. E. Vassalos, **D. Bakalis** and H. T. Vergos, "*On the Use of Double-LSB and Signed-LSB Encodings for RNS*", Proc. of 17th International Conference on Digital Signal Processing (DSP), Corfu, Greece, July 6-8, 2011 (DOI: 10.1109/ICDSP.2011.6004929).
27. E. Vassalos, **D. Bakalis** and H. T. Vergos, "*Modulo 2^n+1 Arithmetic Units with Embedded Diminished-to-Normal Conversion*", Proc. of 14th Euromicro Conference on Digital System Design: Architectures, Methods & Tools (DSD), pp. 468-475, Oulu, Finland, August 31-September 2, 2011 (DOI: 10.1109/DSD.2011.66).
28. E. Vassalos, **D. Bakalis** and H. T. Vergos, "*Configurable Booth-encoded Modulo $2^n\pm 1$ Multipliers*", Proc. of 8th Conference on Ph.D. Research in Microelectronics & Electronics (PRIME), pp. 107-110, Aachen, Germany, June 12-15, 2012.
29. O. Giannou, H. T. Vergos and **D. Bakalis**, "*Squarers in QCA Nanotechnology*", Proc. of 12th International Conference on Nanotechnology (IEEEENANO), Birmingham, UK, August 20-23, 2012 (DOI: 10.1109/NANO.2012.6321897).
30. E. Vassalos, **D. Bakalis** and H. T. Vergos, "*SUT-RNS Residue-to-Binary Converters Design*", Proc. of 15th Euromicro Conference on Digital System Design: Architectures, Methods & Tools (DSD), pp. 65-72, Cesme, Turkey, September 5-8, 2012 (DOI:10.1109/DSD.2012.121).
31. E. Vassalos and **D. Bakalis**, "*On the Design of Modulo 2^n-1 Cubing Units*", Proc. of 23rd Great Lakes Symposium on VLSI (GLSVLSI), pp. 251-256, Paris, France, May 2-3, 2013 (DOI:10.1145/2483028.2483104).
32. E. Vassalos, **D. Bakalis** and H. T. Vergos, "*Reverse Converters for RNSs with Diminished-one Encoded Channels*", Proc. of IEEE Region 8 Conference EUROCON (EUROCON), pp. 1798-1805, Zagreb, Croatia, July 1-4, 2013 (DOI:10.1109/EUROCON.2013.6625221).
33. E. Vassalos and **D. Bakalis**, "*Modulo 2^n-2 Arithmetic Units*", Proc. of IEEE Region 8 Conference EUROCON (EUROCON), pp. 1806-1813, Zagreb, Croatia, July 1-4, 2013 (DOI:10.1109/EUROCON.2013.6625222).
34. E. Vassalos, **D. Bakalis** and H. T. Vergos, "*RNS Assisted Image Filtering and Edge Detection*", Proc. of 18th International Conference on Digital Signal Processing (DSP), Santorini, Greece, July 1-3, 2013 (DOI:10.1109/ICDSP.2013.6622821).

Citations

The publications have been cited by other scientists more than 190 times.

Teaching Courses

- Computer Architecture
- Digital Systems Design with VHDL
- Digital Electronics
- Microprocessors
- Computer Programming I
- Computer Programming II – Laboratory
- Object-oriented Programming